AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

Claim 1 (Canceled).

Claim 2 (Previously Presented): The shift register block as set forth in claim 29, wherein:

the first and second unit circuits are flip-flop circuits.

Claims 3-9 (Canceled).

Claim 10 (Previously Presented): The data signal line driving circuit as set forth in claim 31, wherein:

the sampling section carries out sampling of image data of divided image signals which are generated by dividing the image signal according to an alignment order of the

data signal lines, the sampling section simultaneously carrying out sampling of the image data of the divided image signals.

Claim 11 (Previously Presented): The data signal line driving circuit as set forth in claim 31, wherein:

the image signal is an analog signal.

Claim 12 (Previously Presented): The data signal line driving circuit as set forth in claim 31, wherein:

the image signal is a digital signal.

Claim 13 (Canceled).

Claim 14 (Previously Presented): The display device as set forth in claim 32, wherein:

the data signal line driving circuit and the scanning signal line driving circuit are formed on a substrate on which the pixels are formed.

Claim 15 (Original): The display device as set forth in claim 14, wherein:

the pixels, the data signal line driving circuit, and the scanning signal line driving circuit include active elements, respectively, each of which is made of a polysilicon thin film transistor.

Claim 16 (Original): The display device as set forth in claim 15, wherein:

the active elements are formed on a glass substrate at a process temperature of not more than 600°C.

Claims 17-20 (Canceled).

Claim 21 (Previously Presented): The shift register block as set forth in claim 29, wherein the first unit circuits for the first shift register are disposed linearly with the first circuit.

Claims 22-28 (Canceled).

Claim 29 (Currently Amended): A shift register block comprising:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock

signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits,

wherein:

a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage;

the first circuit comprises [[is]] (i) a processing circuit which uses output of one of the first unit circuits, (ii) a second unit circuit for a second shift register of a system different from a system of the first shift register, and (iii) a processing circuit which uses output of the second unit circuit of the second shift register; and

signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.

Claim 30 (Currently Amended): A signal line driving circuit, comprising:

a shift register block for sequentially outputting a selection signal, so as to drive a plurality of signal lines,

wherein:

the shift register block comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage; the first circuit comprises [[is]] (i) a processing circuit which uses output of one of the first unit circuits, (ii) a second unit circuit for a second shift register of a system different from a system of the first shift register, and (iii) a processing circuit which uses output of the second unit circuit of the second shift register; and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.

Claim 31 (Currently Amended): A data signal line driving circuit comprising:

a sampling section for driving a plurality of data signal lines by sampling image data from an image signal according to a selection signal sequentially outputted from a shift register block so as to transfer the image data to the data signal lines,

wherein:

the shift register block comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage; the first circuit comprises [[is]] (i) a processing circuit which uses output of one of the first unit circuits, (ii) a second unit circuit for a second shift register of a system different from a system of the first shift register, and (iii) a processing circuit which uses output of the second unit circuit of the second shift register; and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.

Claim 32 (Currently Amended): A display device, comprising:

a plurality of data signal lines;

a plurality of scanning signal lines intersecting with the data signal lines;

pixels provided for each pair of the data signal lines and the scanning signal lines;

a scanning signal line driving circuit for driving the scanning signal lines; and

a data signal line driving circuit comprising a sampling section for driving a plurality of data signal lines by sampling image data from an image signal according to a selection signal sequentially outputted from a shift register block so as to transfer the image data to the data signal lines,

wherein:

the shift register block of the data signal line driving circuit comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage; the first circuit comprises [[is]] (i) a processing circuit which uses output of one of the first unit circuits, (ii) a second unit circuit for a second shift register of a system different from a system of the first shift register, and (iii) a processing circuit which uses output of the second unit circuit of the second shift register; and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.

Claim 33 (Currently Amended): A shift register block comprising:

a first shift register comprising a plurality of cascade-connected first unit circuits for sequentially propagating an input signal therethrough in response to a clock signal, the first unit circuits of the first shift register being linearly disposed so that physical spaces are provided between each adjacent pair of first unit circuits; wherein

a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage,

the first circuit comprises [[is]] (i) a processing circuit which uses output of one of the first unit circuits, (ii) a second unit circuit for a second shift register of a system different from a system of the first shift register, and (iii) a processing circuit which uses output of the second unit circuit of the second shift register, and

signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.